What Is Claimed Is:

1. An In-Plane switching mode LCD device, comprising:

a plurality of gate and data lines crossing each other to define a plurality of pixel regions;

a plurality of thin film transistors (TFTs) formed at crossing points of the gate and data lines to be alternately positioned along lower and upper side pixel regions adjacent to corresponding gate lines;

a plurality of storage lines to be parallel with the gate lines, each storage line being separated;

a plurality of pixel electrodes within the pixel regions to be connected to drain electrodes of the TFTs; and

a plurality of common electrodes disposed at fixed intervals from the pixel electrodes and connected to the storage lines.

2. The device according to claim 1, wherein a high-level first common voltage and a low-level second common voltage are alternatively supplied to adjacent storage lines.

3. The device according to claim 2, wherein the first and second common voltages are inversely supplied to corresponding storage lines when a frame is changed.

4. The device according to claim 2, wherein the high-level first common voltage and the low-level second common voltage are synchronized with a gate pulse applied to the gate line corresponding to the storage line.

5. The device according to claim 1, further comprising a dummy line disposed along the lowermost portion of the horizontal gate line or the uppermost portion of the horizontal gate line.

6. The device according to claim 1, wherein the drain electrode of the TFT overlaps the storage line to form a storage capacitor.

7. The device according to claim 1, wherein the storage line is formed along a circumferential portion of the pixel region to be parallel with one of an adjacent gate and data line.

8. The device according to claim 7, wherein the storage line is formed along a corresponding thin film transistor in parallel with the gate line to be elongated to adjacent pixel regions by crossing the data line along one side of the pixel region.

9. The device according to claim 1, wherein the common electrode at least partially overlaps with the storage line.

10. The device according to claim 9, wherein the common electrode overlaps with the storage line at the common electrode portion adjacent to the data line within the pixel region.

11. The device according to claim 1, wherein the storage line includes a first storage line parallel with the gate line along the TFTs, and a second storage line connected to the first storage line in parallel with the data line.

12. The device according to claim 11, wherein the second storage line overlaps with the common electrode along a right side of the pixel region, and the first storage line crosses a left-side data line of the pixel region.

13. The device according to claim 11, wherein the second storage line overlaps with the common electrode along the left side of the pixel region, and the first storage line crosses the right-side data line within the pixel region.

14. The device according to claim 1, wherein the storage line is formed on the same layer as the gate line.

15. The device according to claim 14, wherein the storage line is formed of the same material as the gate line.

16. The device according to claim 1, wherein the pixel electrode is formed in a center portion of the pixel region, and the common electrode is formed along a circumferential portion of the pixel region at a predetermined interval from the pixel electrode.

17. The device according to claim 1, wherein the pixel electrode is formed in parallel with the data line.

18. The device according to claim 1, further comprising a gate driver for alternately supplying first and second common voltages Vcom(+)/Vcom(-) to odd- and even-numbered storage lines, and for supplying a gate driving voltage to the gate lines.

19. The device according to claim 18, wherein the gate driver includes:

a shift register receiving a Gate Start Pulse signal GSP, a Gate Shift Clock signal GSC, and a Left/Right select signal L/R from a processor for shifting the GSC signal and outputting the shifted GSC signal;

a level shifter receiving a Gate Output Enable signal GOE from the processor for sequentially shifting signal levels output from the shift register in response to the GOE signal, and outputting the shifted signal level; and

a buffer receiving a high level VGH, a low level VGL, and first and second common voltages Vcom(+)/Vcom(-) from the processor,

wherein the buffer is synchronized with the signal output from the level shifter to output scanning signals to the gate lines and first and second common voltages to the storage lines.

20. The device according to claim 19, wherein the shift register receives the Left/Right select signal L/R from the processor to perform a both-side shifting function.

21. The device according to claim 19, wherein the buffer alternately supplies the high-level first common voltage and the low-level second common voltage to the storage line corresponding to the gate line when supplying the scanning signal to the gate line.

22. The device according to claim 18, wherein an output terminal of the gate driver further includes a storage line signal supply pin disposed between gate line signal supply pins for supplying the signals to the gate lines.

23. The device according to claim 22, wherein the output terminal of the gate driver further includes two pins for a dummy line at lowermost or uppermost portion of the gate line signal supply pins.

24. The device according to claim 1, further comprising:

a gate driver for sequentially scanning signals to the gate lines, and alternately supplying the low and high level common voltages to the storage lines; and

a source driver for supplying the data voltage for negative fields to the data line of the pixel to which the high level common voltage is supplied, and for supplying the data voltage for positive fields to the data line of the pixel to which the low level common voltage is supplied.

25. The device according to claim 24, wherein the positive field is a data voltage value being larger than value of the low level common voltage, and the negative field is a data voltage value being smaller than a data voltage value of the high level common voltage.

26. The device according to claim 24, wherein the source driver outputs the data voltage for one of the positive fields and the data voltage for one of the negative fields with a gamma standard voltage circuit established by an additional circuit.

27. The device according to claim 24, wherein the source driver includes:

a shift register receiving a Source Start Pulse signal SSP, a Source Shift Clock signal SSC, and a Left/Right select signal L/R from a processor and stores the signals according to respective addresses;

first and second latch parts receiving a Load signal from the processor to receive and store RGB Digital Data signals for even/odd modes in corresponding addresses;

a decoder DAC receiving gamma standard voltages according to one of the positive fields and the negative fields for changing digital signals stored in the first and second latch parts into analog signals; and

an output buffer outputting the respective signals of the decoder according to corresponding data lines.

28. The device according to claim 27, wherein the decoder receives the gamma standard voltages for the positive fields and the negative fields according to a Polarity Out Load (POL) level supplied from the processor.

29. The device according to claim 1, wherein the plurality of storage lines disposed in an offset configuration to be parallel with the gate lines along the TFTs;

30. A liquid crystal display device, comprising

a LCD panel having a plurality of gate and data lines crossing each other to define a plurality of pixel regions, a plurality of pixel electrodes on each pixel region, and a plurality of common lines having a plurality of common electrodes disposed at fixed intervals from the pixel electrodes;

a gate driver for sequentially scanning signals to the gate lines, and supplying the low and high level common voltages to the common lines; and

a source driver for supplying the data voltage for negative fields to the data line of the pixel to which the high level common voltage is supplied, and for supplying the data voltage for positive fields to the data line of the pixel to which the low level common voltage is supplied.

31. An In-Plane switching mode LCD device, comprising:

a plurality of gate and data lines crossing each other to define a plurality of pixel regions;

a plurality of storage lines formed between the gate lines, the storage lines to which first and second common voltages are alternately supplied;

a plurality of first thin film transistors connected to odd-numbered gate lines and even-numbered data lines;

a plurality of second thin film transistors connected to the even-numbered gate lines and the odd-numbered data lines;

a plurality of pixel electrodes in the pixel regions to be connected to drain electrodes of one of the first thin film transistors and the second thin film transistors; and

a plurality of common electrodes in the pixel regions at fixed intervals from the pixel electrodes to be connected to the storage lines.

32. The device according to claim 31, further including:

a plurality of storage capacitors formed between the storage lines adjacent to the drain electrodes of one of the first thin film transistors and the second thin film transistors; and

a plurality of liquid crystal capacitors between the pixel electrodes and the storage lines.

33. The device according to claim 31, wherein the first and second common voltages are alternatively supplied to the storage line when a frame is changed.

34. The device according to claim 31, wherein the first and second common voltages are synchronized with a gate pulse applied to the gate line corresponding to the storage line.

35. The device according to claim 31, further including a dummy line disposed along lowermost or uppermost portion in parallel with the plurality of gate lines.